Inventor: DANIEL J. DOVE

REDUCED PIN-COUNT SYSTEM INTERFACE FOR GIGABIT ETHERNET PHYSICAL LAYER DEVICES

Background of the Invention

The present invention generally relates to computer networking, and more particularly to an interface for physical layer devices operating in a network. The present invention is particularly adapted for use in Gigabit Ethernet physical layer devices.

Those skilled in the art of local area networks (LAN) know that standards define the parameters of communication and vary depending upon the speed and type of operation that is being employed in the system. Even though individual LANs may employ one or more of various standards, they typically use a medium consisting of twisted copper wire pairs for the transmission and reception of data. It is generally a requirement that one or more pairs be used for transmission of data in one direction and one or more other pairs to receive data in the opposite direction.

As is also known to those skilled in the art, it is necessary to have an interface for providing serialized data on the pairs of wires for transmitting and receiving data that may not be in serial form when input to the interfaces. Depending upon the particular standard being used, there may be up to 28 pins of data that are input to the interface for a ten bit

interface (TBI) or a Gigabit media independent interface (GMII) or a media independent interface (MII). These standards are set forth in Institute of Electric and Electronic Engineers (IEEE) standards identified as IEEE802.3u MII and IEEE802.3z GMII and the TBI.

Summary of the Invention

The present invention is directed to a reduced number of input and output pins, i.e., pin-count, that can implement the above GMII and TBI standards, and is hereinafter referred to as the Reduced Gigabit Media Independent Interface (RGMII), which is adapted to also implement a reduced ten bit interface (RTBI). The RGMII is intended to be an alternative to both the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 13 pins in a cost effective and technology independent manner. The RGMII is adapted to map pins to transfer data at the same data rate with control functionality with a minimum number of input and output pins. It does so by utilizing both the rising and falling edges of the clock signal and complies with existing interface specifications set forth in the IEEE standards and utilizes a unique assignment of pins to accomplish optimization in the operation of the interface. To accomplish this optimization, the data paths and all associated control signals are reduced and control signals are multiplexed together and both edges of the clock signal is used. A novel selection of signal assignments optimizes this interface beyond any obvious selection. For example, assigning CRS and COL together allows gigabit implementations which are typically full-duplex to eliminate an additional pin.

Description of the Drawings

FIGURE 1 is a block diagram of the system illustrating the 12 input and output pins to the serializer/deserializer or PHY embodying the present invention.

FIG. 2 is a multiplexing and timing diagram of the system embodying the present invention.

Detailed Description

The signal definitions that apply to the present invention are set forth in the following TABLE 1. The table has four columns, which from left to right indicate the signal name, RTBI mode, RGMII mode and a description of the signals. The signals are signals that are applied or are produced on the pins shown on the left side of a Serializer/Deserializer (SER/DES) shown in FIG. 1. The RGMII shares four data path signals (TD[3:0]) with the Reduced Ten Bit Interface (RTBI) and shares control functionality with a fifth data signal (TX_CTL) in the transmit mode and similar sharing occurs in the receive mode (RD[3:0] and RX_CTL). The transmit clock signal TXC and receive clock signal RXC complete the 12 pins. With the inclusion of the MDIO/MDC serial management signals, the RTBI does not require independent control signals like LK_REF, BYTE_EN, etc. The register assignment of the SER/DES shown in FIG. 1 can be made in various ways by an implementer of the present invention.

With respect to TABLE 1, the TXC signal is the transmit reference clock signal and can be either a 125 Mhz, 25 Mhz or 2.5 Mhz clock signal depending upon the chosen implementation. The RXC signal is a receive reference clock signal and has the same speed values and is derived from the received data stream. The TD signals are provided on four lines that are labeled TD0 - TD3. In the RTBI mode, bits 3:0 are transmitted on the rising edge of the TXC clock signal and bits 5 through 8 are transmitted on the falling edge of the clock signal. In the RGMII mode, bits 3:0 are transmitted on the rising edge of the clock signal and bits 7:4 are transmitted on the falling edge of the clock signal. The signal TX_CTL signal provides some data information as well as control signals. With the RTBI mode, the fifth bit is transmitted on the rising edge of the TXC clock signal and the tenth bit is transmitted on the falling edge of the clock signal. An RGMII mode signal TXEN is transmitted on the rising edge of the clock signal and an error code TXERR is transmitted on the falling edge of the clock signal. As is clear from the table, the received data is assigned to four pins that are similarly defined as are the TD signal and an RX_CTL signal is defined in a manner similar to the TX_CTL signal. The RXDV and RXERR signals are status

signals indicating that the data is either valid or in error. The RXDV signal is applied on the rising edge of the clock signal and the RXERR signal on the falling edge thereof. The CRS signal may be applied on the rising edge of the clock signal and a COL signal on the falling edge thereof for half duplex implementations.

Signal Name	RTBI	RGMII	Description
TXC	MAC	MAC	The transmit reference clock signal will be 125Mhz, +- 50ppm with a maximum peak-peak jitter of 100ps.
TD[3:0]	PCS	MAC	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits 7:4 on ↓ of TXC
TD[4]_TD[9] TXEN_TXERR	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, TXERR on ↓ of TXC
RXC	PHY	PHY	The receive reference clock signal will be 125Mhz, +- 50ppm. (May be derived from TXC)
RD[3:0]	PHY	PHY	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits 7:4 on ↓ of RXC
RD[4] _RD[9] RXDV_ RXERR	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of TXC, RXERR on ↓ of TXC
CRS_ COL	N/A	PHY (OPT*)	CRS on ↑ of TXC, COL on ↓ of TXC (*CRS_COL required for half-duplex implementations only)

TABLE 1

As is clear from the table, it is understood that data and control information is multiplexed by taking advantages of both edges of the reference clock signals and sending the lower four bits on the rising edge and the upper four bits on the falling edge of the clock

signal. Control signals are preferably multiplexed into a single clock cycle using the same technique. The manner in which the multiplexing is carried out is generally indicated in the multiplexing and timing diagram shown in FIG. 2. The transmitted clock signal TXC is shown at 14 and has rising edges 16 and falling edges 18 as indicated. The transmit data signals for the RGMII mode are shown on line 20, where the lower four bits of data are transmitted during the rising edge of the clock signal and bits 7:4 being transmitted at the time of the falling edge of the clock signal 18. With regard to the RTBI mode, it is shown on line 22 where the higher bits 3:0 are also transmitted on the rising edge 16 of the clock signal and bits 8:5 are transmitted at the time of the falling edge 18 of the clock signal. In the RGMII mode, the transmit enable TXEN signal and the transmit error TXERR signals are applied on line 24 with the TXEN signal being applied at the time of the rising edge of the clock signal and TXERR at the time of the falling edge 18 of the clock signal. In the RTBI mode, the line 26 transmits data bit 4 and on the rising edge and bit 9 on the falling edge. The timing of the transmit clock signal received at the receiver is shown on line 28 and is skewed relative to the transmitted data by an amount TskewR which is larger than the amount of skew that is provided of the TXC clock signal of the clocking of the data being transmitted. The critical timing specifics are set forth in Table 3 and include the TskewT (also illustrated in FIG. 2) is the data to clock output skew at the transmitter and as shown in the table, it is within plus or minus 500 picoseconds. The TskewR signal is the data to clock input skew that is measured at the receiver and must be within 1 and 2.8 nanoseconds. As is set forth in the table, this skew will require introducing delay that will be added to the associated clock signal to guarantee that received data has settled down before the clock signal edge arrives in which to sample the data. This is normally done by routing the clock signal on the printed circuit board in such a way to provide the necessary trace delay to comply with the specification. Other items of Table 3 include the clock cycle duration of 7.2 to 8.8 nanoseconds for 2.5 MHz clock signal, as well as the duty cycle and rise and fall times which are relatively self-explanatory and known to those of ordinary skill in the art.

With regard to the signal levels that are use, the RGMII and RTBI signals are

based upon 2.5v CMOS interface voltages, although other implementations may be used. With the preferred implementation, the signal levels are as shown in the following Table 2.

Symbol	Parameter	Conditions	Min	Max	Units
VOH	Output High Voltage	*IOH* = -1.0mA; *VCC* = Min	2.1	VDD+.3	V
VOL	Output Low Voltage	*IOL*=1.0mA; *VCC*=Min	GND-.3	0.40	V
VIH	Input High Voltage	VIH>VIH_*Min*; *VCC*=Min	1.7	–	V
VIL	Input Low Voltage	VIH>VIL_*Max*; *VCC*=Min	-	.70	V
IIH	Input High Current	*VCC*=Max; *VIN* = 2.5V	-	15	µA
IIL	Input Low Current	*VCC*=Max; *VIN* = 0.4V	-15	-	µA

TABLE 2

It is preferred that the timing for this interface will be such that the clock signal and data are generated simultaneously by the source of the signals and therefore skew between the clock signal and data is critical to proper operation. This provides tighter control of skew.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Clock to Data output Skew (at Transmitter)	-500	0	500	ps
TskewR	Clock to Data input Skew (at Receiver) (This implies that PC board design will require clock signals to be routed such that an additional trace delay of greater than 1.5ns will be added to the associated clock signal.)	1.0		2.0	ns
Tcyc	Clock Cycle Duration	7.5	8	8.5	ns
Tpuh	Positive Pulse Width	3.8	4	4.2	ns
Tpul	Negative Pulse Width	3.8	4	4.2	ns
Tr/Tf	Rise / Fall Time (20-80%)			.75	ns

TABLE 3

This present invention can be used to implement the 10/100 Mbps Ethernet Serial Media Independent Interface (SMII) by using TXC, TXD, RXD signals at the 125MHz rate as specified in the SMII version 1.2 document and the SYNCH bit can be multiplexed upon the TXEN signal. Support for SMII version 2.1 may be implemented by using RXCLK for self-synchronous clocking, but it is optional.

The decision about which mode of operation the interface will use is also a matter of choice. It may be done with hard-wired pins, or through register bits that are controlled by software which is easier to implement in an integrated circuit than fixed delay offsets.

From the foregoing it should be understood that a media independent interface has been shown and described which can implement the BMII and TBI standards described herein and which has a reduced number of input and output pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 13 pins in a cost effective and technology independent manner. The RGMII is adapted to map pins to transfer data at the same data rate with control functionality with a minimum number of input and output pins.

While various embodiments of the present invention have been shown and described, it should be understood that other modifications, substitutions and alternatives are apparent to one of ordinary skill in the art. Such modifications, substitutions and alternatives can be made without departing from the spirit and scope of the invention, which should be determined from the appended claims.

Various features of the invention are set forth in the appended claims.